

Consequently, structures or layers formed upon semiconductor layer 20 laterally adjacent to intermediate layer 33 may also be polished to approximately the same elevation level as intermediate layer 33. In this manner, intermediate layer 33 may serve as an additional layer upon which the polishing process may terminate above or within. Fig. 9 illustrates a polishing process, which polishes upper layer 42 to an elevation within layer 34. In such an embodiment, layer 34 may include any material with similar polishing characteristics to those of upper layer 42. For example, layer 34 may include a layer of doped silicon. In such an embodiment, layer 34 may be etched at a faster rate than lateral portions of upper layer 42. Fig. 10 illustrates such an etch process, thereby etching layer 34, underlying 32, and laterally adjacent regions of upper layer 42 to form isolation regions 48. As shown in Fig. 10, step height 50 may be formed due to the different etch characteristics of layer 34 and upper layer 42. The thickness of step height 50 may depend on the thickness of layer 34 and 32 in Fig. 9. As with step height 46 of Fig. 8, step height 50 is preferably less than approximately 200 angstroms above the top of trenches 40. In one embodiment, the upper surface of the remaining portions of upper layer 42 may be less than approximately 50 angstroms above the top of trenches 40. Alternatively, the upper surface isolation regions 48 may be substantially coplanar with the upper surface of semiconductor layer 20 or below the upper surface of semiconductor layer 20 (not shown).

Please replace pg. 24, lines 5-19, with the amended the paragraph below. A "marked-up" version of each amendment is included in **Attachment A**.

Fig. 11 illustrates a polishing process which polishes upper layer 42 subsequent to Fig. 4 to an elevation within layer 32. In such an embodiment, the polishing process may polish through layer 34 or alternatively, layer 34 may have been omitted from the formation of the topography. The entirety of the polished upper surface may then be etched as illustrated in Fig. 12 to form isolation regions 52. In an embodiment in which layer 32 comprises a grown oxide, layer 32 may etch at slightly slower rate than the deposited dielectric material of upper layer 42. As such, a negative step height may result as shown in Fig. 12. More specifically, the upper surface of upper layer 42 may be below the upper surface of semiconductor layer 20. However, step height 54 may be minimal such that laterally adjacent active devices may still be sufficiently isolated. Preferably, the upper surfaces of isolation regions 52 may be less than 200 angstroms below the upper surface of semiconductor layer 20. In one embodiment, the upper surfaces of isolation regions 52 may be less than 50 angstroms below the upper surface of semiconductor layer 20. Alternatively, the upper surfaces of isolation regions 52 may be substantially coplanar with the upper surface of semiconductor layer 20 (not shown).